

What is claimed is:

1. A method comprising:  
receiving an indication of bits of incoming data from a first serial bus;  
buffering the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data;  
during the buffering, detecting whether at least some of the bits indicate a synchronization field.
2. The method of claim 1, further comprising:  
after the buffering, communicating the bits to a second serial bus to form the outgoing data.
3. The method of claim 2, wherein the communicating comprises:  
selectively enabling a transmitter based on the detection.
4. The method of claim 3, further comprising:  
determining whether the indication of the bits indicates valid bit logic levels; and  
further basing enablement of the transmitter on the determination.
5. The method of claim 1, wherein the receiving comprises:  
receiving an indication of at least one analog signal from the first serial bus; and  
converting the indication of said at least one analog signal into indications of at least some of the bits.
6. The method of claim 1, wherein the buffering comprises:  
passing the bits through a delay line.
7. The method of claim 1, wherein the detecting comprises:  
comparing at least some of the bits to an indication of a predetermined bit pattern.

1 8. A repeater comprising:

2 a data recovery circuit to receive an indication of bits of incoming data from a first  
3 serial bus and buffer the bits to accommodate a difference between a first rate of the  
4 incoming data and a second rate of outgoing data; and  
5 a synchronization detection circuit coupled to the data recovery circuit to detect,  
6 while the data recovery circuit buffering the bits, whether at least some of the bits indicate a  
7 synchronization field.

1 9. The repeater of claim 8, further comprising:

2 a transmitter to receive an indication of the bits from the data recovery circuit and use  
3 the indication from the data recovery circuit to communicate the bits to a second serial bus to  
4 form the outgoing data.

1 10. The repeater of claim 9, wherein the synchronization circuit selectively  
2 enables the transmitter based on the detection by the synchronization detection circuit.

1 11. The repeater of claim 10, further comprising:

2 a squelch detection circuit to indicate whether valid bit logic levels are present on the  
3 first serial bus,  
4 wherein the synchronization circuit selectively enables the transmitter further based  
5 on the indication from the squelch detection circuit transmitter.

1 12. The repeater of claim 10, further comprising:

2 an analog-to-digital conversion circuit to receive an analog signal from the first serial  
3 bus and convert the analog signal into an indication of at least some of the bits.

1 13. The repeater of claim 10, wherein the data recovery circuit comprises:

2 a delay line to delay the bits by multiple cycles of a clock signal.

1 14. The repeater of claim 10, wherein the synchronization detection circuit  
2 comprises:  
3 a comparator to compare at least some of the bits to an indication of a predetermined  
4 bit pattern to perform the detection.

1 15. A system comprising:  
2 a first serial bus;  
3 a second serial bus; and  
4 a repeater coupled to the first and second serial busses to receive an indication of bits  
5 of incoming data from the first serial bus, and concurrently buffer the bits to accommodate a  
6 difference between a first rate of the incoming data and a second rate of outgoing data and  
7 detect whether at least some of the bits indicate a synchronization field.

1 16. The system of claim 15, wherein the repeater comprises:  
2 a receiver to receive an indication of bits of the incoming data from the first serial  
3 bus; and  
4 a transmitter to communicate the bits to a second serial bus to form the outgoing data.

1 17. The system of claim 16, further comprising:  
2 a synchronization circuit to detect the synchronization field and selectively enable the  
3 transmitter in response to the detection.

1 18. The synchronization circuit of claim 16, wherein the synchronization detection  
2 circuit comprises:  
3 a comparator to compare at least some of the bits to an indication of a predetermined  
4 bit pattern to perform the detection.

1 19. The system of claim 15, further comprising:  
2 a squelch detection circuit to enable communication to the second serial bus based on  
3 whether valid bit logic levels are present on the first serial bus.

- 1           20.    The system of claim 15, further comprising:  
2            an analog-to-digital conversion circuit to receive an analog signal from the first serial  
3   bus and convert the analog signal into an indication of at least some of the bits.

2025-04-24